

Overview

The IPB-PLAT-XY is an audio IP core for encoding and/or decoding multiple streams of multiple formats on a single device. The system can be customized to include several instances of the processor (CPU), sharing multiple reconfigurable accelerators (REConf).

The IPB-PLAT-XY platform is supported in ASICs and FPGAs (Xilinx or Altera).

The system has a control interface to load programs, issue commands and retrieve status information.

The IPB-PLAT-XY platform requires program and data memories which can be external or embedded in the chip.

The audio data I/O interface can be configured to support multiple industry formats or a simple parallel interface.

Features

- Encodes and/or decodes multiple audio streams in multiple formats
- Programming and control interface using SPI or APB slave interface
- Seamless codec parameter change
- Cycle accurate latency controller ideal for A/V synchronization
- AXI4 master interface to memory controller
- Three boot loading modes
- Multi-channel parallel TDM interfaces (PTDM) and optionally I²S/TDM or SPDIF/AES3

Available Audio Formats

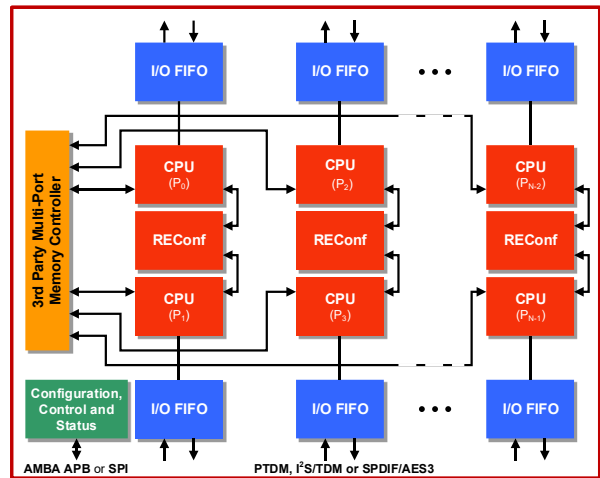
- MPEG-1/2 Layers I/II
- MPEG-2/4 AAC-LC (up to 6 channels)
- MPEG-2/4 HE-AAC (up to 6 channels)
- MPEG-2/4 HE-AAC v2
- AAC XLD

Benefits

- Low power consumption
- Low operation frequency
- Compact hardware implementation

Disclaimer: IPbloq reserves the right to modify the current technical specifications without notice

Block Diagram



Implementation Results for IPB-PLAT-10 (1 CPU, 0 REConf)

FPGA	LUTs	FFs	BRAMs	DSPs
Xilinx Kintex-7	6400	3550	9 x 32K +9 x 16K	4
FPGA	ALMs	Registers	Memory bits	DSPs
Intel Arria V	4200	4130	312000	4
ASIC	Cell count	Embedded RAM (kB)	Power @100 MHz (mW)	
TSMC 65 nm	57750	37.1	20.1	

Deliverables

- Program binary
- Verilog source code or FPGA netlist
- Verilog testbench for RTL simulation
- Synthesis constraints
- Hardware datasheet and software manual
- Evaluation environment or time-limited FPGA netlist (optional)

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