IPB-SPDIF-RX

CONFIGURABLE SPDIF-AES3 RECEIVER

Overview

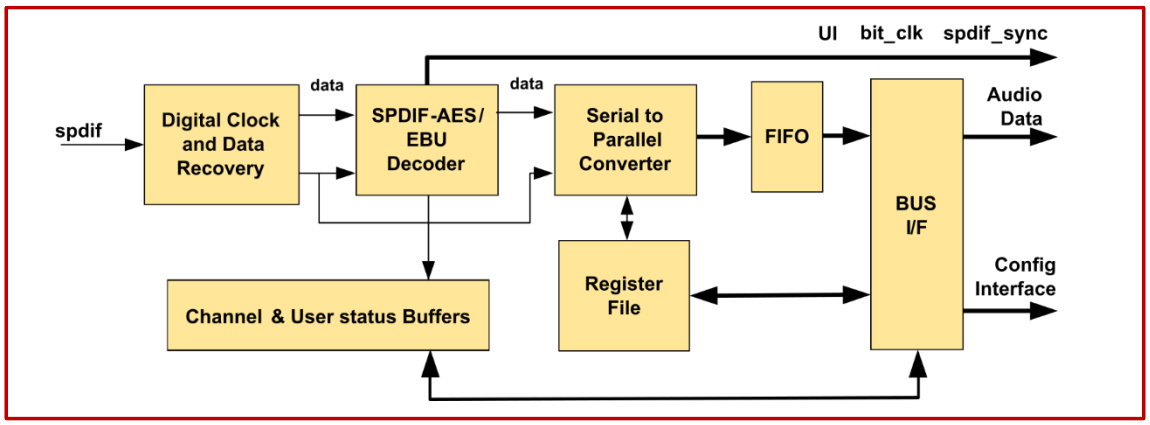
The IPB-SPDIF-RX core is a digital audio receiver supporting the SPDIF (IEC60958) and the AES3 standards for stereo PCM audio transmission, with hardware support for the IEC61937 and SMPTE337M standards for non-PCM multi-channel compressed audio.

Its purely digital clock and data recovery method avoids PLLs, reducing the receiver size and complexity.

Deliverables

- Verilog source code or FPGA netlist
- Verilog testbench for RTL simulation
- Synthesis constraints
- Datasheet
- Example software driver

Block Diagram



Features

- Supports the SPDIF (IEC60958) and AES3 standards for stereo PCM audio transmission
- Supports the IEC61937, SMPTE 337M standards for non-PCM audio transmission (Dolby Digital, AAC, DTS, MPEG, etc.)
- Digitally de-jitters recovered clock and outputs a good quality audio retransmission clock
- Automatic removal of stuffing bits in non-PCM mode
- Average 0.6/Fs lock time
- System clock (fclk) minimum required frequency F_{fclk} = 420*Fs for Fs = 96 kHz or lower, and F_{fclk} = 640*Fs for Fs = 192 kHz
- Optional Channel Status and User bits memory mapped buffers
- Programmable FIFO level trigger
- Configurable endianness for both control and data interfaces
- Automatically detects input signal sample rate

Disclaimer: IPbloq reserves the right to modify the current technical specifications without notice

Implementation results

Xilinx FPGAs	Slices	LUTs	Registers
Spartan-6™	417	2023	1258
Virtex-6™	315	1921	1264

ASICs	Cell count
TSMC 45 nm	17515

Benefits

- Fully digital solution without PLL
- Small silicon area

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