IPB-MPEG-SD

MPEG-1/2 – Layer I/II Audio Decoder

Overview

The **MPEG-1/2 – Layer I/II Audio Decoder** (IPB-MPEG-SD) is an audio IP core for decoding up to two stereo audio streams in real-time.

It is designed to run on our IPB-PLAT audio engine platform, which may support encoding and decoding of multiple streams in multiple formats on a single device.

The IPB-MPEG-SD software requires an instance of the IPB-PLAT audio engine platform named **IPB-PLAT-10**. This instance contains only one processor.

The user can upload the IPB-MPEG-SD program using a hardware interface. The program can be configured, run and monitored by means of a configuration, control, and status register file, accessed by the same control interface.

The audio input and output interfaces include a native parallel interface. Other interfaces, such as, I^2S/TDM and SPDIF/AES3 are also available.

Features

- MPEG-1/2 - Layer I/II decoders are compliant with ISO/IEC 11172-3 and 13818-3 audio standards, using Fraunhofer IIS high quality software
- Supported channel modes: mono, dual mono, stereo, and joint stereo
- Supported sampling rates: 16, 22.05, 24, 32, 44.1 and 48 kHz
- 16 to 24-bit output audio resolution
- Requires 550 kB of external memory
- Configurable output latency useful to synchronize with other sources (e.g. video)
- Minimum latency: 1 frame assuming burst data input
- Software interface protocol for control, configuration and monitoring
- Parameter change while muting or repeating one frame
- Real time operation @40 MHz (80 MHz for two audio streams)

(1) Implementation results for other FPGAs or ASIC technologies can be provided upon request

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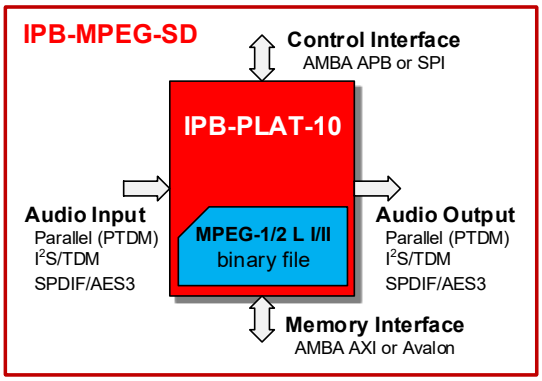
Benefits

- Compact hardware implementation – fits economically in FPGAs and ASICs
- Low operation frequency
- Low power consumption

Block Diagram



Implementation Results(1)

Intel/Altera Cyclone-V

ALMs	Registers	DSPs	Memory bits
4,100	4,080	4	312,000

Xilinx Spartan-6

LUTs	FFs	DSPs	BRAM 18K
6,400	3,550	4	22

Deliverables

- Program binary
- Software manual
- Hardware datasheet
- RTL of FPGA netlist
- Implementation constraints

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