IPB-ASRC-H

24-BIT -130DB MULTI-CHANNEL ASYNCHRONOUS SAMPLE RATE CONVERTER

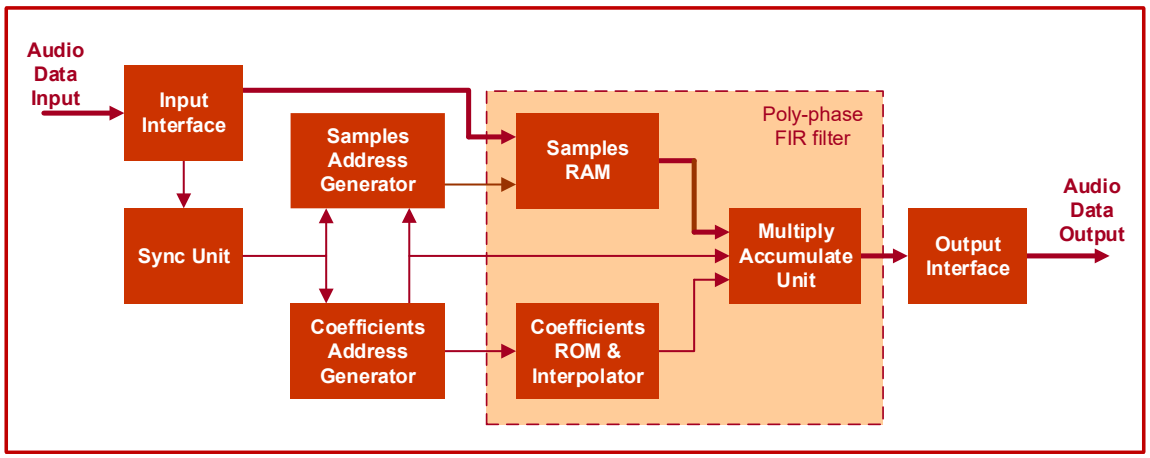
Overview

The IPB-ASRC-H belongs to a family of Multi-Channel Asynchronous Sample Rate Converters (ASRCs). This IP core can be used in systems on chip for consumer or professional audio applications. It has been designed for systems requiring very high quality in terms of harmonic distortion and noise, tolerance and rejection of input jitter.

Benefits

- Eliminates the need for a discrete SRC chip
- Supported in both FPGA and ASIC
- Customizable architecture allows features to be modified upon request (e.g. higher number of channels, different conversion ratios, different quality/resources tradeoffs)

Block Diagram



Features

- Fully digital IP core
- 2-channel audio SRC expandable up to 128 audio channels (upon request)
- Sample size: up to 24 bits
- Automatically adjusts to input and output sample rate changes
- Input and output sample rate range: 8 kHz to 192 kHz
- Sampling rate conversion ratios from 1 : 7.5 to 7.5 : 1
- Available audio interfaces: multi-channel TDM serial/parallel audio, I²S, AES3/SPDIF (pre-configured with only one interface)
- Tolerates and rejects input jitter
- Latency: $64/FS_{IN} + 2/FS_{OUT}$
- -130 dB THD+N for common conversion ratios
- Fast synchronization time: 128 input sample periods

Disclaimer: IPbloq reserves the right to modify the current technical specifications without notice

FPGA	ALM	REG	M10K	DSP
Arria-V	870	1420	32	12

FPGA	Slices	RAM18	DSP
Spartan-6	700	16	6

ASIC	Cell count	ROM	RAM
TSMC 45nm	15900	8192x28	256x24

Deliverables

- Verilog source code or FPGA netlist
- Verilog testbench for RTL simulation
- Synthesis constraints
- Datasheet

Contact Information

Web: www.ipbloq.com

Email: info@ipbloq.com

Address: Av. Reinaldo dos Santos, 23-4º dto
2675-674 Odivelas
Portugal