IPB-AAC-LC-SE

AAC-LC STEREO AUDIO ENCODER

Overview

The **AAC-LC Stereo Audio Encoder** (IPB-AAC-LC-SE) is a software IP for encoding one stereo stream in AAC-LC format. It is designed to run on our IPB-PLAT audio engine platform, which may support encoding and decoding of multiple streams in multiple formats on a single device.

The IPB-AAC-LC-SE software requires an instance of the IPB-PLAT audio engine platform named **IPB-PLAT-10**. This instance contains only one processor.

The user can upload the IPB-AAC-LC-SE program using a hardware interface. The program can be configured, run and monitored by means of a configuration, control, and status register file, accessed by the same control interface.

The audio input and output interfaces include a native parallel interface. Other interfaces, such as, I^2S/TDM and SPDIF/AES3 are also available.

Features

- AAC-LC encoders are compliant with the ISO/IEC 13818-7 audio standard, using Fraunhofer IIS high quality software
- Supported transport types: ADIF, LATM/LOAS and ADTS (with ARIB support and CRC)
- Supported channel modes: mono, stereo and dual mono
- Supported sample rates: 11.025, 12, 16, 22.05, 24, 32, 44.1 and 48 kHz
- 16-bit input audio resolution
- Requires 1,2 MB of external memory
- Configurable latency (minimum: 1 frame) useful to synchronize with other sources (e.g. video)
- Software interface protocol for commands, configuration and monitoring
- Parameter change while muting or repeating one frame
- Real time operation @80 MHz

(1) Implementation results for other FPGAs or ASIC technologies can be provided upon request

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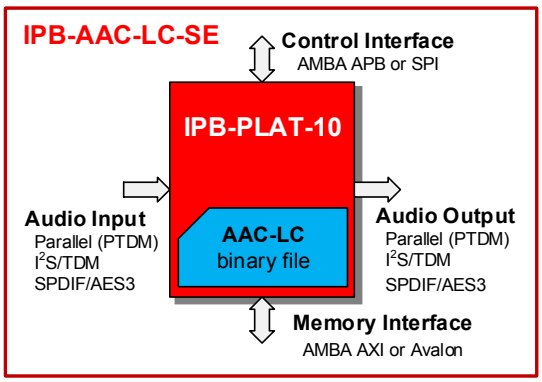
Benefits

- Compact hardware implementation – fits economically in FPGAs and ASICs
- Low operation frequency
- Low power consumption
- Small external memory footprint

Block Diagram



Implementation Results(1)

Intel/Altera Cyclone-V

ALMs	Registers	DSPs	Memory bits
4,100	4,080	4	312,000

Xilinx Spartan-6

LUTs	FFs	DSPs	BRAM 18K
6,400	3,550	4	22

Deliverables

- Program binary
- Software manual
- Hardware datasheet
- RTL or FPGA netlist
- Implementation constraints

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